1. A method of forming insulating material alignment posts associated with active device structures comprising:

providing a silicon semiconductor wafer having patterned said active device therein and thereon; and

forming said insulating material alignment posts in a pattern over said pattern of active device structures.

2. A method according to Claim 1 wherein said optical interference layer improves the reflectivity of the said metallic mirror.

3. The method of claim 1 wherein said optical interference multilayer stack is formed by the process of plasma-enhanced chemical vapor deposition.

4. The method of claim 1 wherein said optical interference multilayer stack is composed of the materials formed by the process of plasma-enhanced chemical vapor deposition.

5. A method according to Claim 1 wherein said optical interference layer is between about 1000 Angstroms and 10000 Angstroms in total thickness.

6. A method according to Claim 1 wherein said alignment posts are placed on the said silicon wafer, realizing micro-display pixels.

7. A method according to Claim 1 for building the said alignment posts to a height from 0.3 microns to 5 microns on the resulting liquid-crystal-on-silicon micro-display.

8. A method of forming a device structure that combines insulating materials for alignment posts and optical interference layers associated with an active device structure in a silicon body comprising:

providing a silicon semiconductor wafer having a pattern of active device structures therein and thereon;

forming a first metallic layer there over;

forming a silicon-oxide insulation layer over the said first metallic layer;

forming a second metallic layer over the said silicon oxide layer, which is used both for connections and for bonding pads;

forming a silicon dioxide insulation over the said second metal layer;

forming a third metallic layer thereover;

forming a photoresist mask over the said third metallic layer having a covering over the planned pixel

locations of the said liquid-crystal-on-silicon display device;

removing the said third metallic layer not covered by the said photoresist mask;

removing the said photoresist mask to provide that each said pixel retains said metallic layer, which shall act as a mirror reflector for the light incident upon said liquid-crystal-on-silicon display device;

depositing the said optical interference layers of silicon oxide/silicon nitride/silicon oxide/silicon nitride over said third metallic layer and said silicon oxide layer.

9. The method of claim 8 wherein said alignment posts are formed by the process of silicon dioxide by wet etching upon the said silicon substrate.

10. The method of claim 9 for forming a silicon dioxide layer of thickness between about 0.1 to 5 microns to achieve the desired height of the alignment posts.

11. The method of claim 9 for forming a photoresist mask over the said silicon oxide layer to cover the location of each planned alignment post.

12. The method of claim 9 for removing the said silicon oxide layer to form the said alignment posts with a wet

etch (such as HF or buffered HF), and removing the said photoresist mask.

13. The method of claim 8 wherein said alignment posts are formed by the process of amorphous silicon by plasma etching upon the said silicon substrate.

14. The method of claim 13 for forming an amorphous silicon layer of thickness between about 0.1 and 5 microns to achieve the desired height of the alignment posts.

15. The method of claim 13 for forming a photoresist mask over the said amorphous silicon layer to cover the location of each planned alignment post.

16. The method of claim 13 for removing the said amorphous silicon to form the said alignment posts by plasma etch, and removing the said photoresist mask.

17. The method of claim 8 wherein said alignment posts are formed by the process of silicon nitride by plug filling upon the silicon substrate.

18. The method of claim 17 for forming a PECVD oxide layer of thickness between 0.1 and 5 microns to achieve the desired height of the alignment posts.

19. The method of claim 17 for forming a photoresist mask over the said PECVD oxide layer to expose the location of each planned alignment post.

20. The method of claim 17 for forming post cavities by plasma etching of the said PECVD oxide layer.

21. The method of claim 17 for plasma enhanced chemical vapor deposition of silicon nitride into the said post cavities.

22. The method of etch-back removal of said silicon nitride, except that silicon nitride deposited in the said post cavities.

23. The method of claim 17 for removing the PECVD oxide layer by wet etch (such as HF or buffered HF) to form the said silicon nitride alignment posts, and removing the said photoresist mask.

24. The method of claim 8 wherein said alignment posts are formed by the process of insulation material by lift-off upon the said optical interference layer OIL.

25. The method of claim 24 wherein a photoresist or PMMA acylic layer of thickness between about 1 and 5 microns is deposited upon the OIL and covered by silicon monoxide

via thermal evaporation, followed by another photoresist layer of thickness between about 0.1 and 1 micron.

26. The method of claim 24 wherein a photomask is used to form the said cavities in the said silicon monoxide by a CF4 plasma etching of the silicon monoxide, after which the silicon monoxide serves as a mask for an oxygen plasma etching of the said two-micron bottom photoresist

27. The method of claim 24 for forming an insulation material by plug filling the cavities formed in the silicon monoxide and two-micron bottom photoresist layer; several insulation materials are available from which to choose, including calcium fluoride, silicon monoxide, yttrium oxide, and aluminum oxide, and the like.

28. The method of claim 24 for removing said bottom photoresist layer by lift-off with an ultrasonic bath, leaving the said alignment posts.

29. The method of claim 8 wherein said alignment posts are formed by the process of polyimide by photosensitive etching upon the OIL.

30. The method of claim 29 for forming a photosensitive polyimide layer of thickness between about 0.1 and 5

microns to achieve the desired height of the alignment posts.

31. The method of claim 29 for exposing the said photosensitive polyimide at the location of each planned alignment post.

32. The method of claim 29 for developing and removing the said photosensitive polyimide to leave the said alignment posts in the location of the exposed polyimide described herein, and removing the said photoresist mask.

33. A device structure that combines insulating materials for alignment posts associated with an active device structure in a silicon body.

34. A device structure that combines insulating materials for alignment posts and optical interference layers associated with an active device structure in a silicon body comprised of:

a silicon semiconductor wafer having a pattern of said active device structures therein and thereon;

pixels on said semiconductor wafer and the whole structure being covered with an optical interference layer;

bonding pads on the said silicon body having wire attached and said wire connected to external contacts for the control logic and power;

liquid crystal material located in the valleys below the peaks of the alignment posts;

glass cover placed upon and supported by the alignment posts to encapsulate the said liquid crystal material, but not over the area outside the liquid-crystal material where the bonding pads are located.

35. A structure according to Claim 34 wherein the alignment posts are made by means of photolithography rather than pre-formed glass beads or rods.

36. A structure according to Claim 34 that contains the said optical interference layers in addition to the said alignment posts.

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